26.6 An 800MHz to 5GHz Software-Defined Radio Receiver in 90nm CMOS

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A software-defined radio (SDR) can tune to any frequency band, select any reasonable channel bandwidth, and detect any known modulation. While progress has been made on DSP and baseband functions for SDR, the low-power radio front-end has remained elusive.

An ADC at the antenna which digitizes all bands simultaneously with equal fidelity will not be practical in the foreseeable future. Today's mobile SDR receiver needs a wideband, linear RF front-end that can be tuned to any *one* channel at a time in the band from 800MHz to 5GHz. This should be followed by a filter with a passband that is tunable over several decades by a clock. The filter should enable the channel of interest to be digitized at the required SNR for acceptable demodulation, whereas adjacent channels can be digitized at any SNR because eventually they are eliminated by a digital filter. The RF front-end and analog filter should limit the DR presented to the ADC input, and allow sampling of the signals at a reasonable rate to achieve power dissipation consistent with mobile requirements. On the other hand, as much as possible, the ADC and DSP should relieve the analog front-end from the traditional burdens of variable gain and filtering. To serve the gamut of cellular and WLAN standards, the ADC should be reconfigurable; for instance, GSM reception needs 14b DR in a 200kHz bandwidth and 10MHz sample rate, whereas 802.11g reception needs a DR of 8b across the Nyquist band at 40MHz rate.

The receiver reported here is designed from the perspective of the ADC to be an efficient RF signal conditioner (Fig. 26.6.1). It comprises an LNA spanning a passband of 400MHz to 5GHz [1], and an LO generator that tunes to important bands in this range. There is no RF preselect filter before or after the LNA. A complex mixer downconverts the channel of interest to zero or low IF. The wanted channel is surrounded by many unwanted channels and bands. The analog filter enables the ADC to sample this wideband spectrum at the rates given above without contaminating the channel of interest centered at DC or low IF with aliases that become co-channel interferers.

An integrate-and-dump, or windowed integration sampler, is best suited to this purpose [2]. This circuit filters its continuous-time input by a *sinc* function prior to sampling, with nulls in its transfer function at all multiples of the sample frequency (Fig. 26.6.1). The circuit is realized by a transconductor, capacitors, and switches. Practically achievable null depth is limited to about 55dB [4], which is not enough for strong adjacent channels. A passive-RC filter with two programmable real poles at the preceding mixer's load assists in this role. The initial sample rate (f_s) must be high enough so that the passive filter is able to provide the required attenuation to the limited depth of the sampler's first null. This rate is then decimated with anti-aliasing passive switched-capacitor FIR filters [3]. Decimation factors and filtering can be configured to suppress in-band and out-of-band channels that will alias on to the desired channel. Signals that lie in the filter sidelobes will alias on to adjacent unwanted channels, but this is of no consequence so long as they do not overload the ADC. The filter's discrete-time sampled-and-held analog output is directly digitized.

The LNA circuit (Fig. 26.6.2) uses a common-gate stage to provide a wideband impedance match and to amplify the input in-phase, and a parallel common-source stage amplifies it in anti-phase. With the same gains in both stages, noise of the common-gate stage is cancelled when the two outputs are sensed differentially [1]. This decouples noise and impedance match, leading to total NF of 3dB or less over the wide passband. The input port and output loads are embedded into maximally flat LC-ladder filters. Gain can be lowered at the expense of noise by disabling the common-source stage, and by dumping signal current. The LNA uses thick-oxide FETs to operate at 2.5V for high linearity.

The mixers must have high gain, large IP2 and IP3, and low flicker noise. The preferred embodiment is a passive FET mixer that is capacitively coupled to an RF transconductor and is connected to a common-gate output stage with low impedance (Fig. 26.6.3). Sensitivity to flicker noise at the gate and offsets is zero if there is no voltage swing at the source/drain of the mixer FETs. This also improves IP2. The loads of the common-gate realize two passive RC poles with switch-selectable R and C.

Mixing with LO harmonics must be suppressed in an SDR receiver. Commutation by a square wave downconverts RF inputs at the LO frequency to zero IF, as well as inputs at the 3rd and the 5th harmonics. When the receiver is tuned to a low band (~900MHz), unwanted signals at the harmonics (~2.7 and 4.5GHz) also enter the receiver. Downconversion by LO harmonics may be suppressed by multiplying the input with a sine wave; however, the conversion gain is poor. High gain mixing ideally free of 3rd and 5th harmonics is realized by adding the outputs of three switching mixers scaled in the ratio 1:√2:1, driven by square waves 45° delayed in phase [5] (Fig. 26.6.3). Errors in the phases result in spurious response.

The clock frequency f_s that determines the filter's integration window is dictated by the blocking template in the band of interest and signal levels in adjacent bands. For example, WCDMA cellular transmissions in the 1.9GHz band become strong blockers for WLAN communications in the 2.4GHz band. It is found by trial and error that the cascade of a discrete-time pole at a fraction of f_s, a $sinc^2$ FIR filter that decimates by 4, and a *sinc* FIR filter that decimates by 3 or 2 is sufficient for almost all practical cases (Fig. 26.6.4). Notches in the filter response are required at multiples of the final sample rate. The discrete-time FIR filters are realized with passive switched-capacitors, while an unswitched capacitor at the transconductor output realizes the pole. All clock phases are generated on-chip. Capacitor mismatch in the time-interleaved channels gives rise to spurious response, while the transconductor's finite output resistance limits null depth. Variable gain of 30dB at baseband is embedded in the windowed integrator by switch-selectable unit transconductors and binary capacitor arrays; this is sufficient to handle the DR of all cellular bands with no need for a dedicated VGA.

The wideband LO generator needs two VCOs: a 3.6GHz differential VCO with 20% tuning range, and a 5GHz quadrature VCO with 10% tuning range. A divide-by-4 circuit after the 3.6GHz VCO generates multiple phases for harmonic-suppression mixing. A divide-by-2 circuit generates quadrature phases to tune the 1.8GHz band. The 5GHz VCO with divide-by-2 tunes the 2.4GHz band. The VCOs use switched amplitude control. Multiplexers and a buffer tree route the selected LO output to the mixers. This LO generator covers all widely used cellular and WLAN bands; continuous coverage can be obtained across the full receiver passband with two additional VCOs.

Implemented in a 90nm CMOS process, the receiver chip size is 2.9×2.4mm² (Fig. 26.6.7). Figure 26.6.5 summarizes the key receiver parameters. The on-chip receiver selectivity at 900MHz is sufficient for GSM and at 2.4GHz for 802.11g WLAN (Fig. 26.6.6). Mixer nonlinearity limits tolerance to blockers. For example, with a -15 dBm WCDMA blocker present, the receiver is desensitized by 4dB to achieve IIP3 of -3.5dBm. New more linear wideband mixer circuits are needed to tolerate larger blockers.

References:

[1] S. Chehrazi, *et al*., "A 6.5 GHz Wideband CMOS Low Noise Amplifier for Multi-Band Use," *IEEE CICC Proc.*, pp. 801-804, Sept., 2005.
[2] J. Yuan, "A Charge Sampling Mixer with Embedded Filter Function for Wireless Applications," *Intl. Conf. on Microwave and Millimeter Wave Tech.*, pp. 315-318, Sept., 2000.
[3] R. B. Staszewski *et al*., "All-Digital TX Frequency Synthesizer and Discrete-time Receiver for Bluetooth Radio in 130-nm CMOS," *IEEE J. of Solid-State Circuits*, vol. 39, no. 12, pp. 2278-2291, Dec., 2004.
[4] A. Mirzaie *et al.*, "A Second-Order Anti-Aliasing Prefilter for an SDR Receiver", *IEEE CICC Proc.*, pp. 629-632, Sept., 2005.
[5] J. A. Weldon *et al.*, "A 1.75GHz Highly-Integrated Narrow-Band CMOS Transmitter with Harmonic-Rejection Mixers," *ISSCC Dig. Tech. Papers*, pp. 160-161, Feb., 2001.

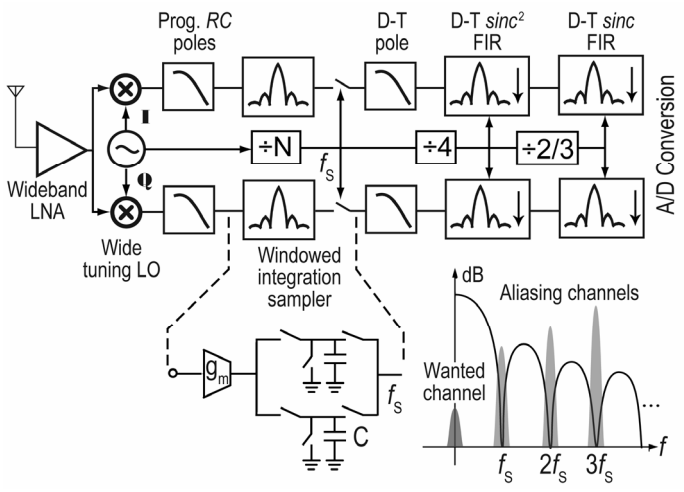

Figure 26.6.1: Receiver block diagram showing baseband anti-alias sampler.

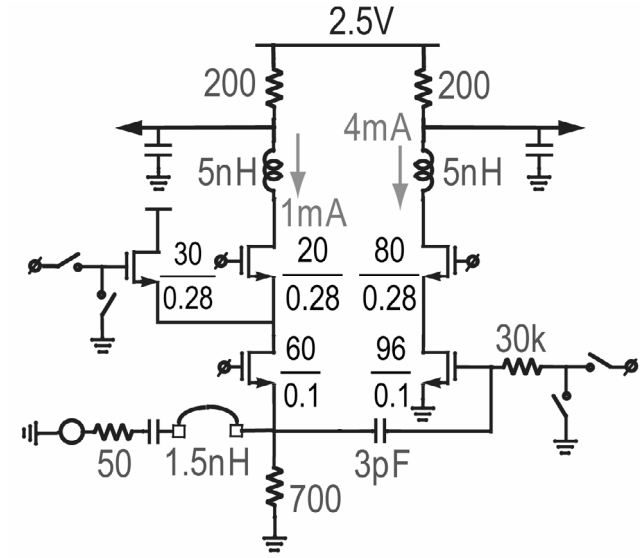

Figure 26.6.2: Wideband LNA.

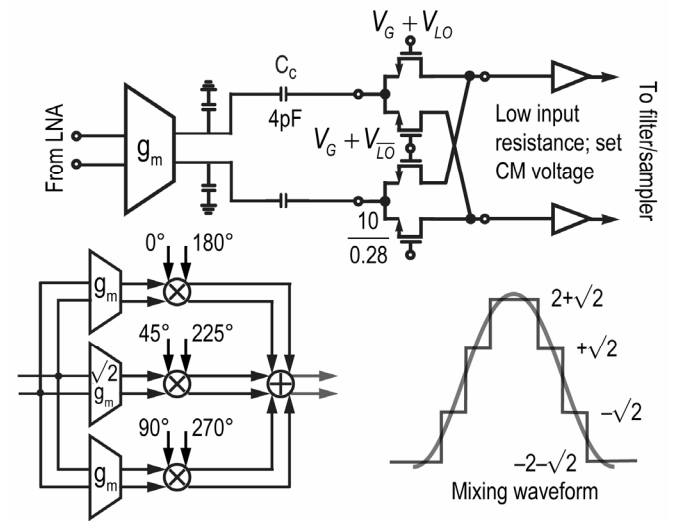

Figure 26.6.3: Mixer circuit and harmonic-suppression method.

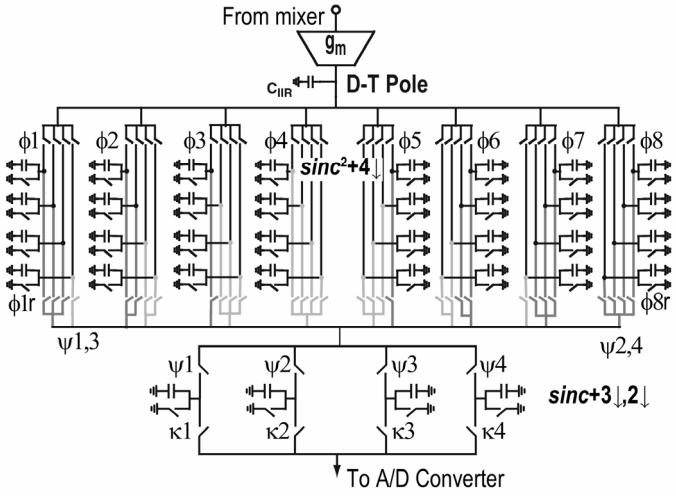

Figure 26.6.4: Baseband sampler and filter circuit.

Current consumption			
Circuit		Supply (V)	Current (mA)
LNA		2.5	5.0
Mixer		2.5	6.4
Filter	GSM (High gain)	1	23.0
	GSM (Low gain)	1	8.0
	802.11g (High gain)	1	28.0
	802.11g (Low gain)	1	13.0
3.8 GHz VCO		1	12.5
Div-by-4		1	6.0
Div-by-2		1	3.0

Gain Ranges	LNA+Mixer (dB)	Filter (dB)
GSM	36 ~ 8	36 ~ 6
802.11g	30 ~ 3	26 ~ –4

Spurious Responses		dB
Mixer	3rd LO harmonic	–38
	5th LO harmonic	–40
Filter (GSM)	Gain at 4.7 MHz	–74
Filter (802.11g)	Gain at 22 MHz	–60

	GSM (dB)	802.11g (dB)
Cascade NF	5	5.5
	NF constant from 10 kHz IF up	
s_{11} (800 MHz~6 GHz)		–10

GSM Linearity	Cascade IIP3 (dBm)	Cascade IIP2 (dBm)
Max. input signal	–3.5	
6 MHz mod. Blocker		+45 ~ +65

Figure 26.6.5: Measured receiver characteristics.

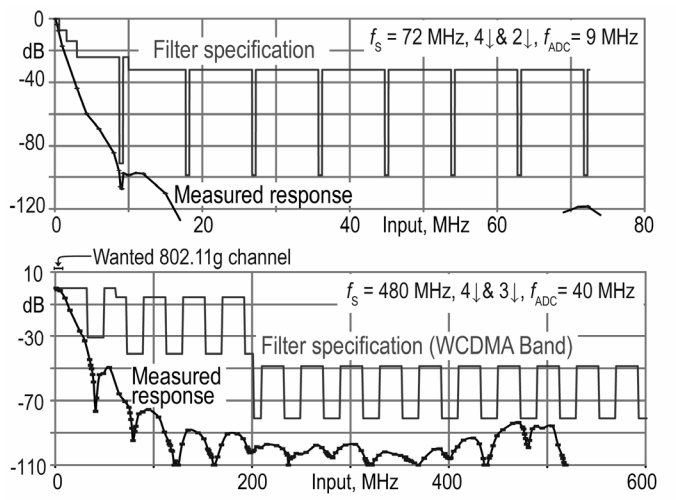

Figure 26.6.6: Measured selectivity in GSM and 802.11g modes.

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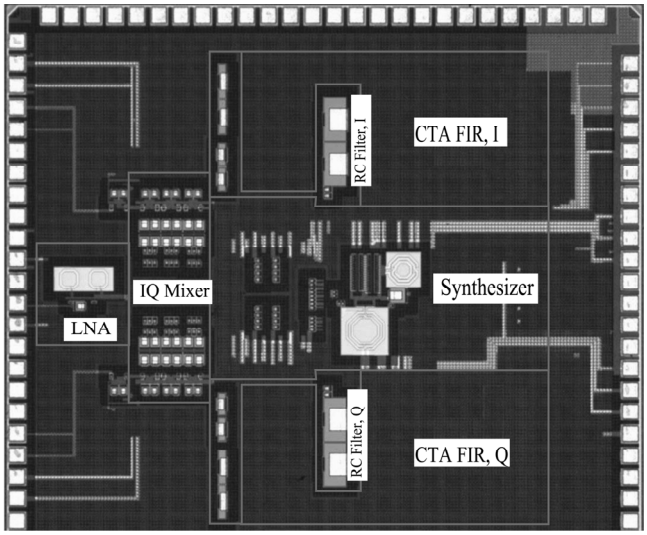

Figure 26.6.7: Chip micrograph.

